Implementing the Design

Introduction

This lab continues with the previous lab. You will perform static timing analysis. You will implement the design with the default settings and generate a bitstream. Then you will open a Hardware Manager and program the FPGA. Since the on-board UART port is dedicated to the PS section of the Zynq chip it is not accessible from the PL section directly. You will use the PmodUSBUART module and connect to one of the PMOD connector JA on the ZedBoard or PMOD connector JE on the Zybo.

Objectives

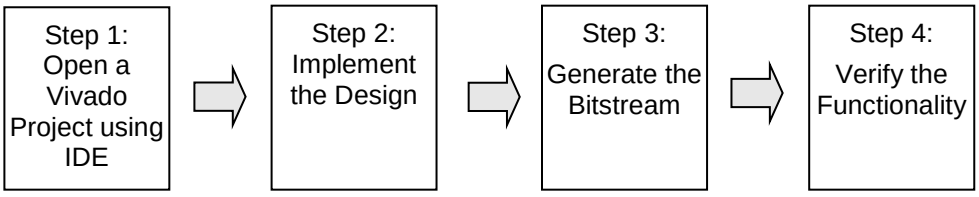
After completing this lab, you will be able to:

- Implement the design
- Generate various reports and analyze the results
- Run static timing analysis
- Generate bitstream and verify the functionality in hardware

Procedure

This lab is broken into steps that consist of general overview statements providing information on the detailed instructions that follow. Follow these detailed instructions to progress through the lab.

General Flow



Open a Vivado Project using IDE — Step 1

1-1. Launch Vivado and open the lab2 project. Save the project as lab3 in the *<2014_2_zynq_labs>* directory making sure that the create subdirectory option is selected. Set the synthesis settings to Rebuild Hierarchy.

> References to **<2014_2_zynq_labs>** is a placeholder for the **c:\xup\fpga_flow\2014_2_zynq_labs** directory and **<2014_2_zynq_sources>** is a placeholder for the **c:\xup\fpga_flow\2014_2_zynq_sources** directory.
>
> Reference to **<board>** means either the **ZedBoard** or the **Zybo**.

1-1-1. Start the Vivado if necessary and open either the lab2 project (lab2.xpr) you created in the previous lab or the lab2 project in the labsolution directory using the **Open Project** link in the Getting Started page.

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1-1-2. Select **File > Save Project As …** to open the *Save Project As* dialog box. Enter **lab3** as the project name. Make sure that the *Create Project Subdirectory* option is checked, the project directory path is **<2014_2_zynq_labs>** and click **OK.**

1-1-3. Click on the **Synthesis Settings** in the *Flow Navigator* pane.

1-1-4. Make sure that the *flatten_hierarchy* is set to **rebuilt**, which allows the design hierarchy to be flattened for synthesis, and then rebuilt which is more useful for design analysis because many logical references will be maintained.

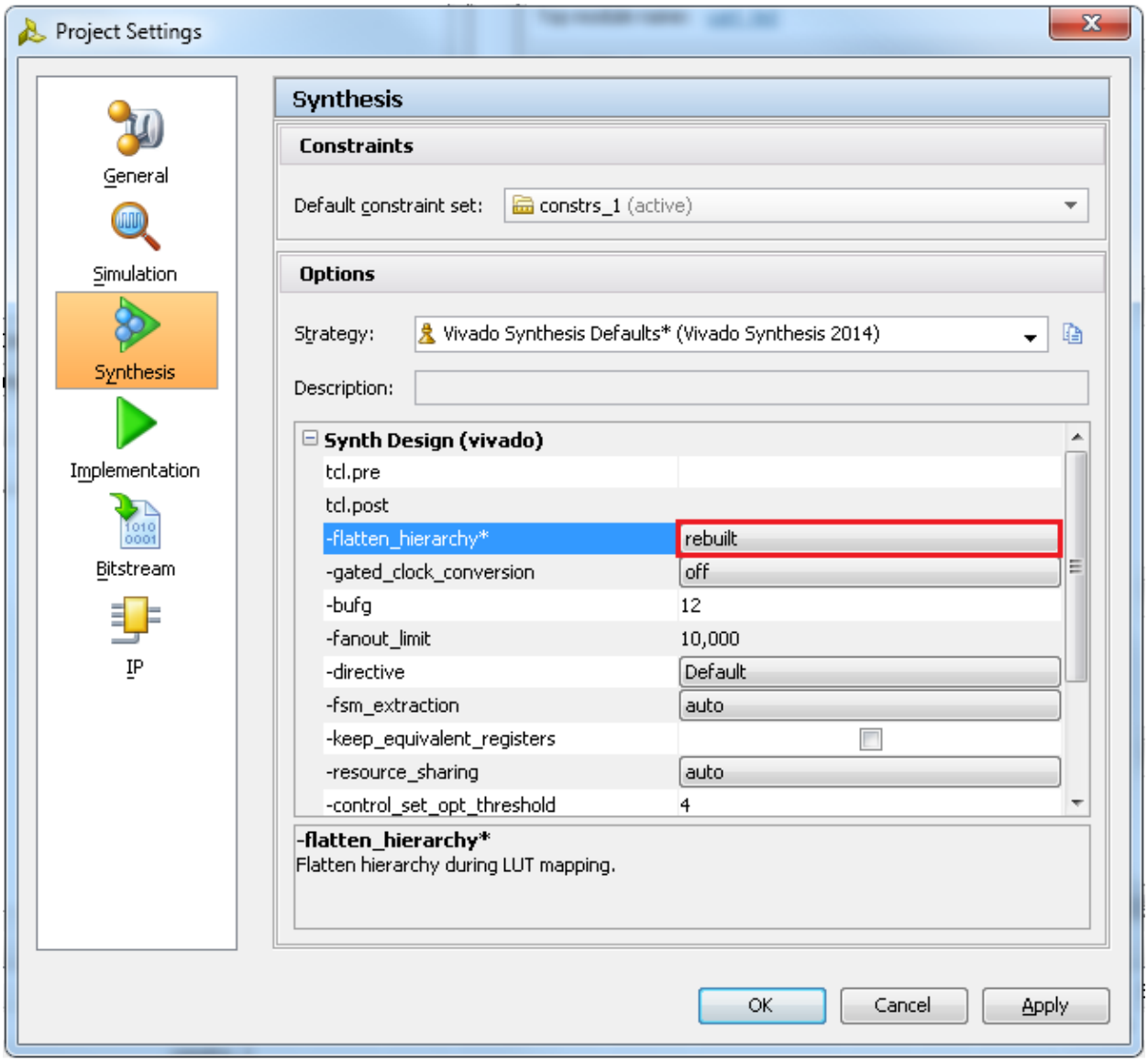

Figure 1. Setting hierarchy to rebuild

1-1-5. Click **OK**.

A Create New Run dialog box will appear asking you if a new run should be created. Click **Yes** and then **OK** to create the new run with **synth_2** name.

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1-2. Synthesize the design. Generate the timing summary and analyze the design.

1-2-1. Click on **Run Synthesis** under the *Synthesis* tasks of the *Flow Navigator* pane.

The synthesis process will be run on the uart_led.v and all its hierarchical files. When the process is completed a *Synthesis Completed* dialog box with three options will be displayed.

1-2-2. Select the *Open Synthesized Design* option and click **OK** as we want to look at the synthesis output.

Click **Yes** to close the elaborated design if the dialog box is displayed.

1-2-3. Click on **Report Timing Summary** under the *Synthesized Design* tasks of the *Flow Navigator* pane.

1-2-4. Leave all the settings unchanged, and click **OK** to generate a default timing report, *timing_1.*

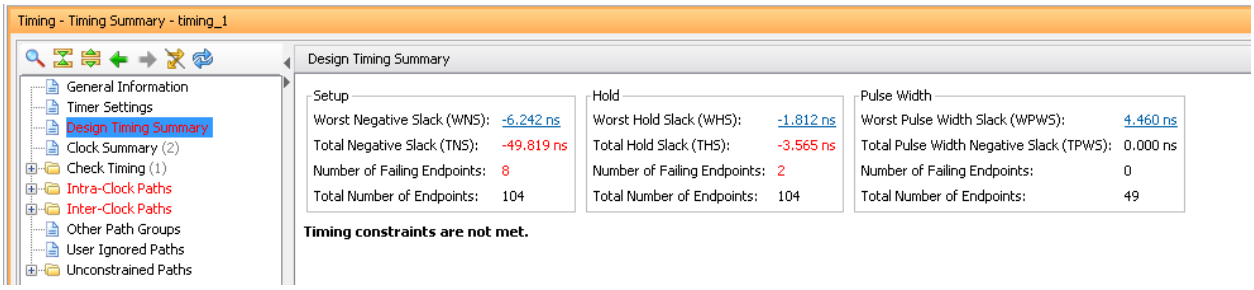

Figure 2. Timing report for the ZedBoard

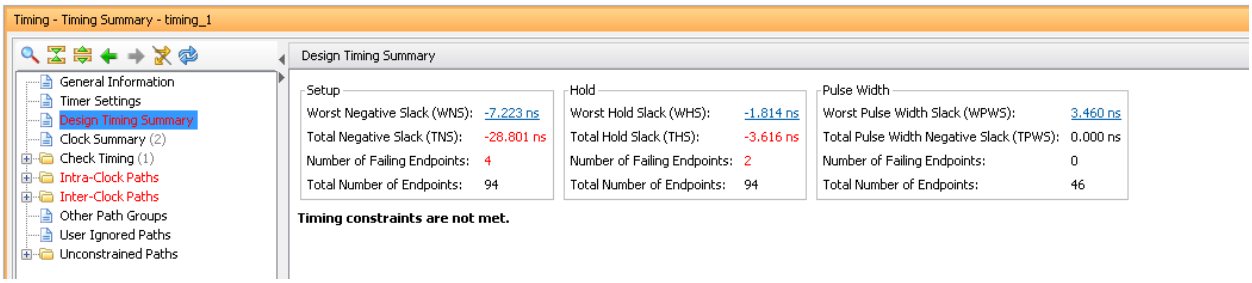

Figure 2. Timing report for the Zybo

1-2-5. Click on the link beside the **Worst Negative Slack** (WNS) and see the failing paths.

1-2-6. Double-click on the Path 23 to see a detailed view of the path. The path report shows four sections: (i) Summary, (ii) Source Clock Path, (iii) Data Path, and (iv) Destination Clock Path.

1-2-7. Select Path 23 in the timing summary panel, or the Path summary view, right-click, and select **Schematic**.

The schematic for the output data path will be displayed.

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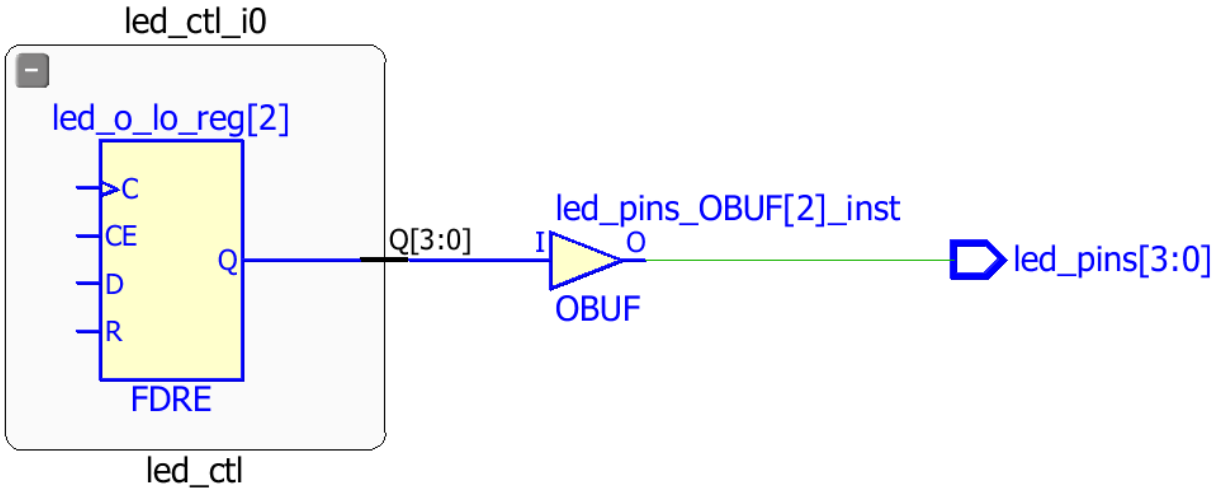

Figure 3. The output data path

1-2-8. In order to see how the Source Clock Path is made up in schematic form, double-click on left end of the C pin of the FDRE in the schematic.

This will show the net between the BUFG and C port of the FDRE.

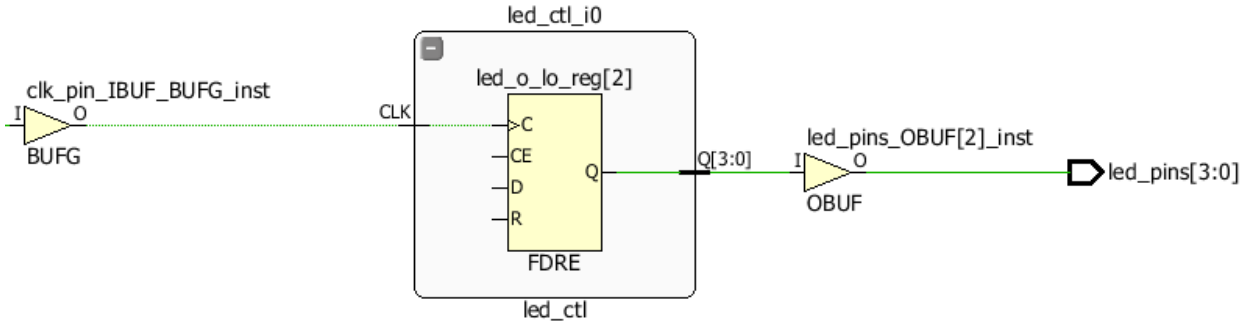

Figure 4. Source to clock port of the FDRE

1-2-9. Similarly, double-click on the left end of the BUFG to see the path between IBUF and BUFG.

1-2-10. Finally, double-click on the input pin of IBUF to see the path between the clock input pin and the IBUF.

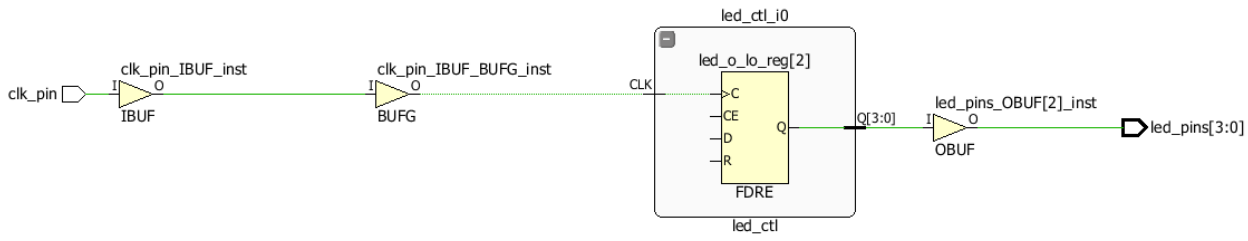

Figure 5. The schematic view of the source clock path

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This corresponds to the Source Clock Path in the timing report.

Source Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock clk_pin rise edge)	(r) 10.000	10.000		
	(r) 0.000	10.000	Site: Y9	clk_pin
net (fo=0)	0.000	10.000		clk_pin
			Site: Y9	clk_pin_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 1.490	11.490	Site: Y9	clk_pin_IBUF_inst/O
net (fo=1, unplaced)	0.800	12.290		clk_pin_IBUF
				clk_pin_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.101	12.391		clk_pin_IBUF_BUFG_inst/O
net (fo=48, unplaced)	0.800	13.191		led_ctl_i0/CLK
				led_ctl_i0/led_o_reg[4]/C

Figure 6. The source clock path for the ZedBoard

Source Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock clk_pin rise edge)	(r) 8.000	8.000		
	(r) 0.000	8.000	Site: L16	clk_pin
net (fo=0)	0.000	8.000		clk_pin
			Site: L16	clk_pin_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 1.491	9.491	Site: L16	clk_pin_IBUF_inst/O
net (fo=1, unplaced)	0.800	10.291		clk_pin_IBUF
				clk_pin_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.101	10.392		clk_pin_IBUF_BUFG_inst/O
net (fo=45, unplaced)	0.800	11.192		led_ctl_i0/CLK
				led_ctl_i0/led_o_reg[1]/C

Figure 6. The source clock path for the Zybo

Since the virtual clock is slower than the clk_pin period, the data path delay includes the clock period of the clk_pin clock source. For the ZedBoard, the virtual clock is set to 12 ns while the clock period is 10 ns. For the Zybo, it is 9 ns and 8 ns respectively.

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Source Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock clk_pin rise edge)	(r) 10.000	10.000		
	(r) 0.000	10.000	Site: Y9	clk_pin
net (fo=0)	0.000	10.000		clk_pin
			Site: Y9	clk_pin_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 1.490	11.490	Site: Y9	clk_pin_IBUF_inst/O
net (fo=1, unplaced)	0.800	12.290		clk_pin_IBUF
				clk_pin_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.101	12.391		clk_pin_IBUF_BUFG_inst/O
net (fo=48, unplaced)	0.800	13.191		led_ctl_i0/CLK
				led_ctl_i0/led_o_reg[4]/C

Data Path

Delay Type	Delay	Cumulative	Location	Logical Resource
FDRE (Prop_fdre_C_Q)	(r) 0.518	13.709		led_ctl_i0/led_o_reg[4]/Q
net (fo=1, unplaced)	0.800	14.509		led_pins_OBUF[4]
			Site: V22	led_pins_OBUF[4]_inst/I
OBUF (Prop_obuf_I_O)	(r) 3.708	18.217	Site: V22	led_pins_OBUF[4]_inst/O
net (fo=0)	0.000	18.217		led_pins[4]
			Site: V22	led_pins[4]
Arrival Time		18.217		

Destination Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock virtual_clock rise edge)	(r) 12.000	12.000		
ideal clock network latency	0.000	12.000		
clock pessimism	0.000	12.000		
clock uncertainty	-0.025	11.975		
output delay	-0.000	11.975		
Required Time		11.975		

Figure 7. Worst failing path for the ZedBoard

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Source Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock clk_pin rise edge)	(r) 8.000	8.000		
	(r) 0.000	8.000	Site: L16	clk_pin
net (fo=0)	0.000	8.000		clk_pin
			Site: L16	clk_pin_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 1.491	9.491	Site: L16	clk_pin_IBUF_inst/O
net (fo=1, unplaced)	0.800	10.291		clk_pin_IBUF
				clk_pin_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.101	10.392		clk_pin_IBUF_BUFG_inst/O
net (fo=45, unplaced)	0.800	11.192		led_ctl_i0/CLK
				led_ctl_i0/led_o_reg[1]/C

Data Path

Delay Type	Delay	Cumulative	Location	Logical Resource
FDRE (Prop_fdre_C_Q)	(r) 0.496	11.688		led_ctl_i0/led_o_reg[1]/Q
net (fo=1, unplaced)	0.800	12.488		led_pins_OBUF[1]
			Site: M15	led_pins_OBUF[1]_inst/I
OBUF (Prop_obuf_I_O)	(r) 3.710	16.198	Site: M15	led_pins_OBUF[1]_inst/O
net (fo=0)	0.000	16.198		led_pins[1]
			Site: M15	led_pins[1]
Arrival Time		16.198		

Destination Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock virtual_clock rise edge)	(r) 9.000	9.000		
ideal clock network latency	0.000	9.000		
clock pessimism	0.000	9.000		
clock uncertainty	-0.025	8.975		
output delay	-0.000	8.975		
Required Time		8.975		

Figure 7. Worst failing path for the Zybo

1-3. Change the design constraint to constrain the virtual clock period to 10 ns for the ZedBoard or 8ns for the Zybo. Re-synthesize the design and analyze the results.

1-3-1. Click **Edit Timing Constraints** under the Synthesized Design.

The Timing Constraints GUI will appear, showing the design has two create clocks, four inputs, and one output constraints. It also shows the constraints in the text form in the All Constraints section.

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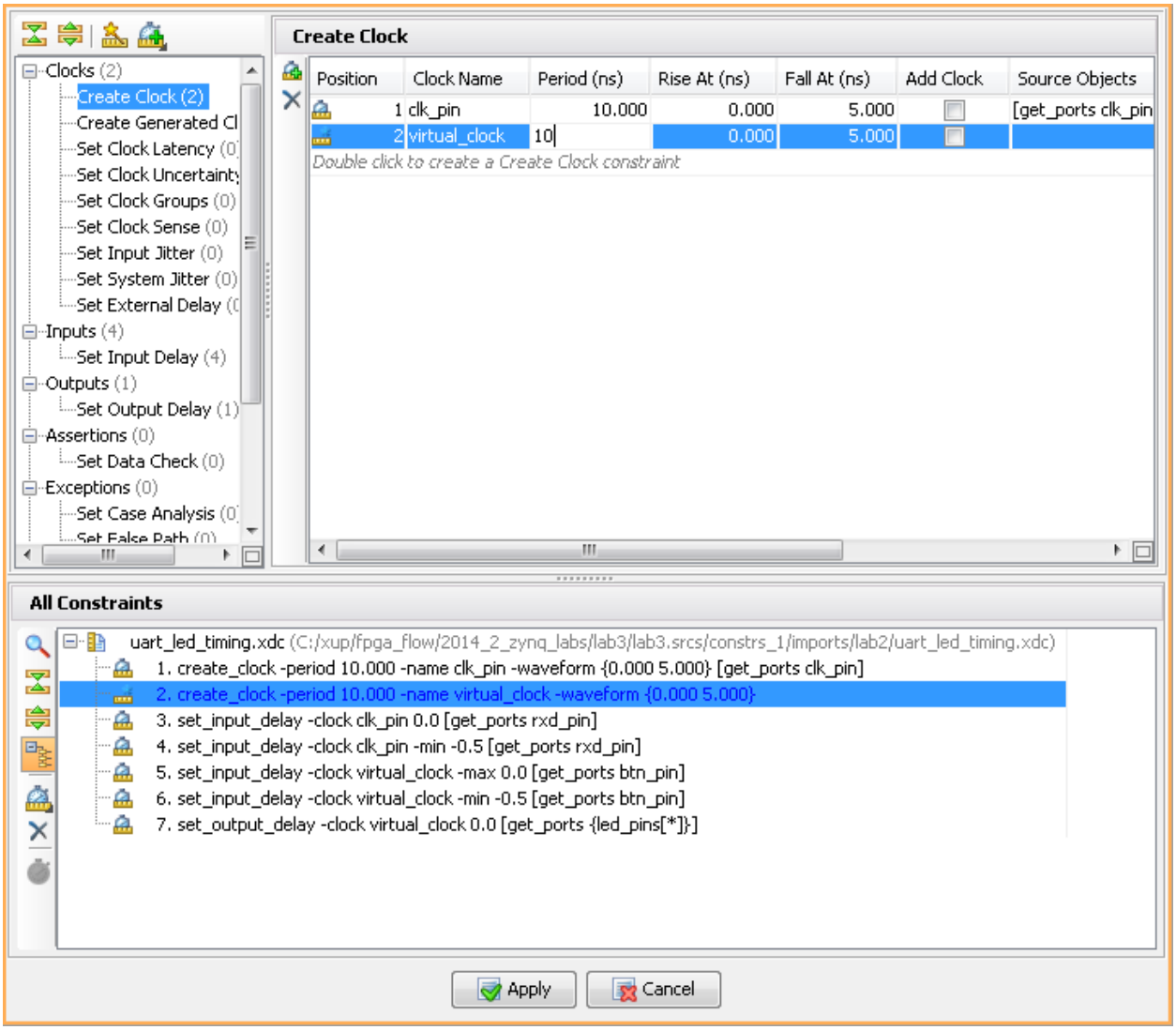

Figure 8. Timing Constraints editor for the ZedBoard

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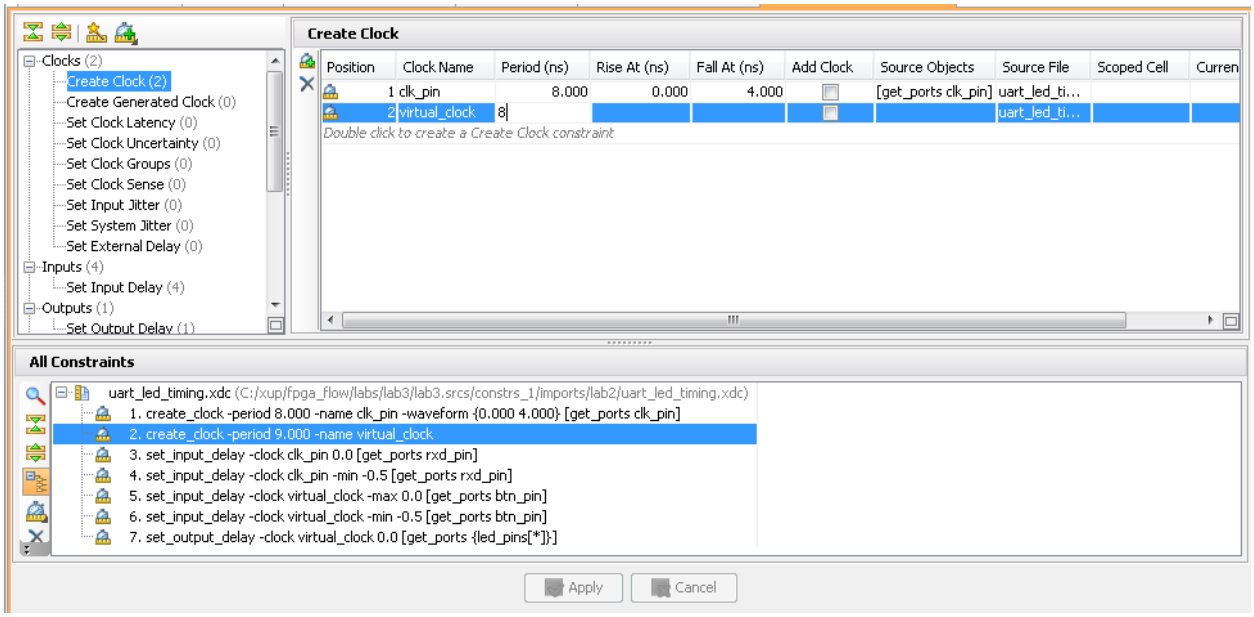
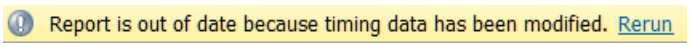


Figure 8. Timing Constraints editor for the Zybo

1-3-2. Click in the **Period** cell of the *virtual_clock* and change the period from **12** to **10** for the **ZedBoard** or **9** to **8** for the Zybo.

1-3-3. Click **Apply**.

Note that since the timing constraint has changed, a warning message in the console pane is displayed to rerun the report.



1-3-4. Click on **Rerun**.

Notice that the WNS is now recalculated.

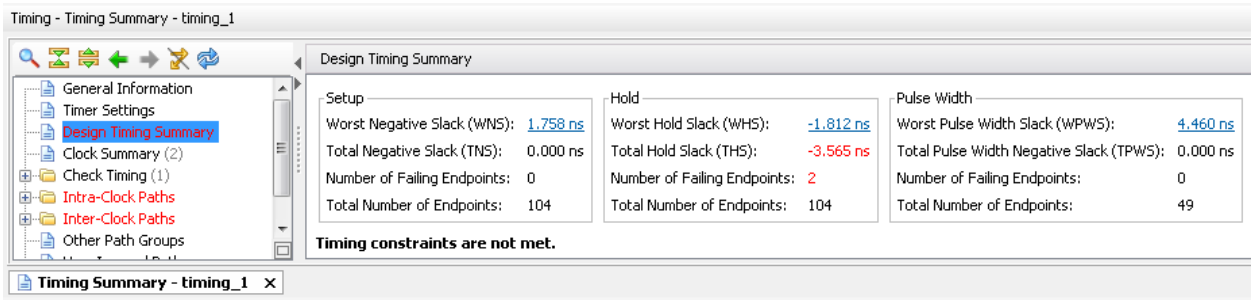


Figure 9. WNS recalculated timing for the ZedBoard

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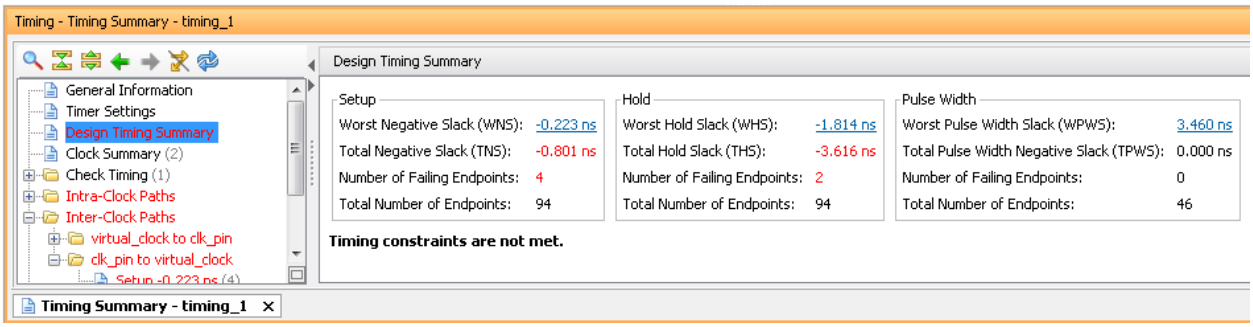

Figure 9. WNS recalculated timing for the Zybo

The WNS has been dramatically reduced but not eliminated for the Zybo. On the ZedBoard, it is entirely gone.

1-3-5. Click on the WNS link again to see the paths.

1-3-6. Double-click on the first path to see the timing compositions.

Notice that the clock source path now does not include the clock period.

Source Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock clk_pin rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000	Site: Y9	clk_pin
net (fo=0)	0.000	0.000		clk_pin
			Site: Y9	clk_pin_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 1.490	1.490	Site: Y9	clk_pin_IBUF_inst/O
net (fo=1, unplaced)	0.800	2.290		clk_pin_IBUF
				clk_pin_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.101	2.391		clk_pin_IBUF_BUFG_inst/O
net (fo=48, unplaced)	0.800	3.191		led_ctl_i0/CLK
				led_ctl_i0/led_o_reg[4]/C

Data Path

Delay Type	Delay	Cumulative	Location	Logical Resource
FDRE (Prop_fdre_C_Q)	(r) 0.518	3.709		led_ctl_i0/led_o_reg[4]/Q
net (fo=1, unplaced)	0.800	4.509		led_pins_OBUF[4]
			Site: V22	led_pins_OBUF[4]_inst/I
OBUF (Prop_obuf_I_O)	(r) 3.708	8.217	Site: V22	led_pins_OBUF[4]_inst/O
net (fo=0)	0.000	8.217		led_pins[4]
			Site: V22	led_pins[4]
Arrival Time		8.217		

Destination Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock virtual_clock rise edge)	(r) 10.000	10.000		
ideal clock network latency	0.000	10.000		
clock pessimism	0.000	10.000		
clock uncertainty	-0.025	9.975		
output delay	-0.000	9.975		
Required Time		9.975		

Figure 10. Source clock path for the ZedBoard

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Source Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock clk_pin rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000	Site: L16	clk_pin
net (fo=0)	0.000	0.000		clk_pin
			Site: L16	clk_pin_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 1.491	1.491	Site: L16	clk_pin_IBUF_inst/O
net (fo=1, unplaced)	0.800	2.291		clk_pin_IBUF
				clk_pin_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.101	2.392		clk_pin_IBUF_BUFG_inst/O
net (fo=45, unplaced)	0.800	3.192		led_ctl_i0/CLK
				led_ctl_i0/led_o_reg[1]/C

Data Path

Delay Type	Delay	Cumulative	Location	Logical Resource
FDRE (Prop_fdre_C_Q)	(r) 0.496	3.688		led_ctl_i0/led_o_reg[1]/Q
net (fo=1, unplaced)	0.800	4.488		led_pins_OBUF[1]
			Site: M15	led_pins_OBUF[1]_inst/I
OBUF (Prop_obuf_I_O)	(r) 3.710	8.198	Site: M15	led_pins_OBUF[1]_inst/O
net (fo=0)	0.000	8.198		led_pins[1]
			Site: M15	led_pins[1]
Arrival Time		8.198		

Destination Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock virtual_clock rise edge)	(r) 8.000	8.000		
ideal clock network latency	0.000	8.000		
clock pessimism	0.000	8.000		
clock uncertainty	-0.025	7.975		
output delay	-0.000	7.975		
Required Time		7.975		

Figure 10. Source clock path for the Zybo

Notice that the clock path delay does not include the entire clock period.

1-3-7. Select **File > Save Constraints.** Click **OK.**.

Notice that the Synthesis Out-of-Date status is displayed on the top-right corner.

Implement the Design Step 2

2-1. Run the implementation after saving the synthesis run. Perform the timing analysis.

2-1-1. In the Design Runs tab, right-click on the synth_2 and select **Reset Runs**. Make sure all generated files are deleted and click **Reset**.

2-1-2. Click the **Close Design** button in the status bar. If prompted, do not save anything.

2-1-3. Click on the **Run Implementation** in the *Flow Navigator* pane.

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2-1-4. Click **OK** when prompted to run the synthesis first before running the implementation process.

When the implementation is completed, a dialog box will appear with three options.

2-1-5. Select the *Open Implemented Design* option and click **OK**. If prompted, close the synthesized design.

2-2. View the amount of FPGA resources consumed by the design using Report Utilization.

2-2-1. In the *Flow Navigator* pane, select **Implemented Design** > **Report Utilization**.

The Report Utilization dialog box opens.

2-2-2. Click **OK**.

The utilization report is displayed at the bottom of the Vivado IDE. You can select any of the resources on the left to view its corresponding utilization.

2-2-3. This time, click Chart (rather than table) and select one of the resources (e.g. Slice Logic) to view how much and which module consumes the resource.

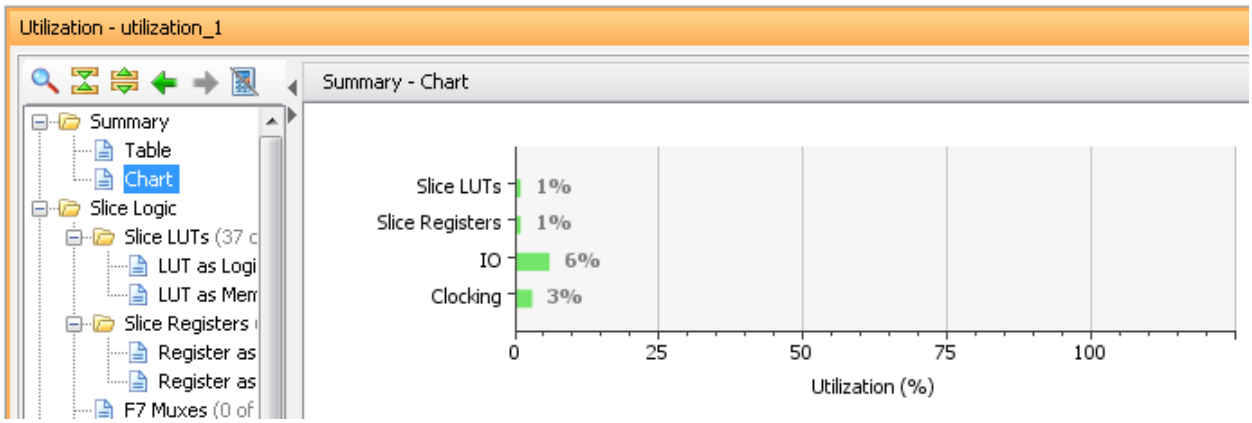

Figure 11. Resource utilization chart for the ZedBoard

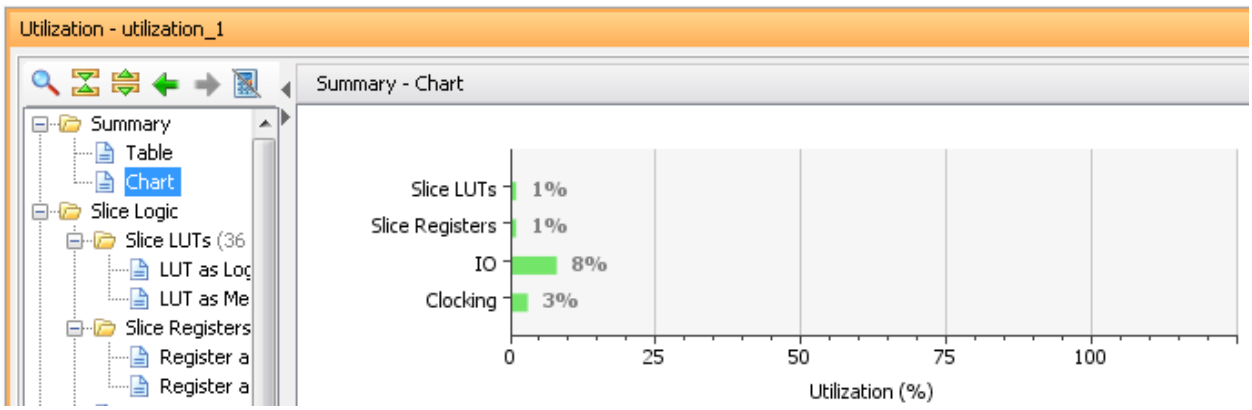

Figure 11. Resource utilization chart for the Zybo

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2-3. Generate a timing summary report.

2-3-1. In the Flow Navigator, under Implementation > Implemented Design, click **Report Timing Summary**

The Report Timing Summary dialog box opens.

2-3-2. Leave all the settings unchanged and click **OK** to generate the report.

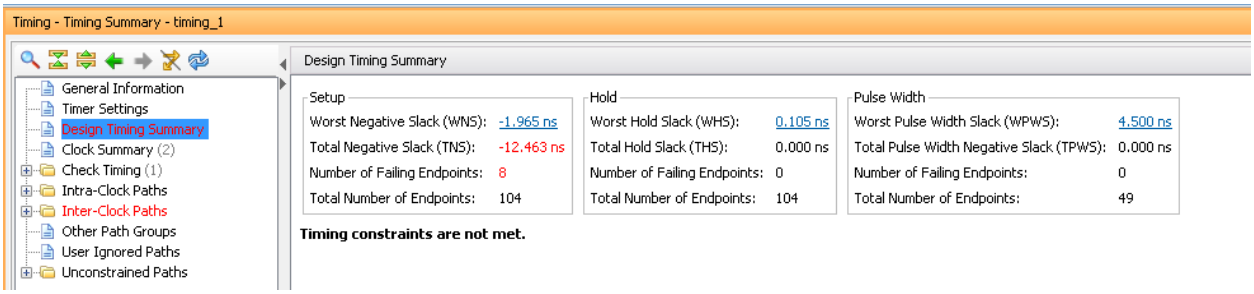

Figure 12. The timing summary report showing timing violations for the ZedBoard design

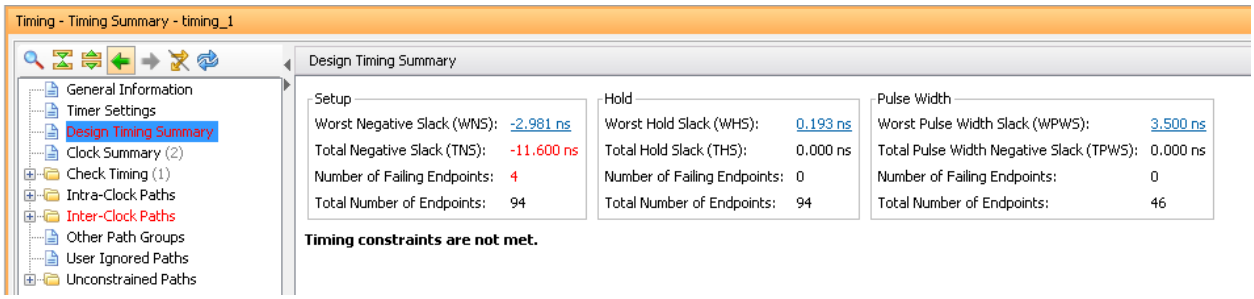

Figure 12. The timing summary report showing timing violations for the Zybo design

2-3-3. Click on the WNS link to see a detailed report to determine the failing path entries.

2-3-4. Double-click on the first failing path to see why it is failing.

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Source Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock clk_pin rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000	Site: Y9	clk_pin
net (fo=0)	0.000	0.000		clk_pin
			Site: Y9	clk_pin_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 1.490	1.490	Site: Y9	clk_pin_IBUF_inst/O
net (fo=1, routed)	2.171	3.661		clk_pin_IBUF
			Site: BUFGCTRL_X0Y0	clk_pin_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.101	3.762	Site: BUFGCTRL_X0Y0	clk_pin_IBUF_BUFG_inst/O
net (fo=48, routed)	1.861	5.623		led_ctl_i0/CLK
			Site: SLICE_X113Y23	led_ctl_i0/led_o_reg[3]/C

Data Path

Delay Type	Delay	Cumulative	Location	Logical Resource
FDRE (Prop_fdre_C_Q)	(r) 0.456	6.079	Site: SLICE_X113Y23	led_ctl_i0/led_o_reg[3]/Q
net (fo=1, routed)	2.330	8.410		led_pins_OBUF[3]
			Site: U21	led_pins_OBUF[3]_inst/I
OBUF (Prop_obuf_I_O)	(r) 3.530	11.940	Site: U21	led_pins_OBUF[3]_inst/O
net (fo=0)	0.000	11.940		led_pins[3]
			Site: U21	led_pins[3]
Arrival Time		11.940		

Destination Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock virtual_clock rise edge)	(r) 10.000	10.000		
ideal clock network latency	0.000	10.000		
clock pessimism	0.000	10.000		
clock uncertainty	-0.025	9.975		
output delay	-0.000	9.975		
Required Time		9.975		

Figure 13. First failing path delays for the ZedBoard

Source Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock clk_pin rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000	Site: L16	clk_pin
net (fo=0)	0.000	0.000		clk_pin
			Site: L16	clk_pin_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 1.491	1.491	Site: L16	clk_pin_IBUF_inst/O
net (fo=1, routed)	1.860	3.351		clk_pin_IBUF
			Site: BUFGCTRL_X0Y16	clk_pin_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.101	3.452	Site: BUFGCTRL_X0Y16	clk_pin_IBUF_BUFG_inst/O
net (fo=45, routed)	1.740	5.192		led_ctl_i0/CLK
			Site: SLICE_X43Y93	led_ctl_i0/led_o_reg[3]/C

Data Path

Delay Type	Delay	Cumulative	Location	Logical Resource
FDRE (Prop_fdre_C_Q)	(r) 0.419	5.611	Site: SLICE_X43Y93	led_ctl_i0/led_o_reg[3]/Q
net (fo=1, routed)	1.663	7.274		led_pins_OBUF[3]
			Site: D18	led_pins_OBUF[3]_inst/I
OBUF (Prop_obuf_I_O)	(r) 3.682	10.956	Site: D18	led_pins_OBUF[3]_inst/O
net (fo=0)	0.000	10.956		led_pins[3]
			Site: D18	led_pins[3]
Arrival Time		10.956		

Destination Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock virtual_clock rise edge)	(r) 8.000	8.000		
ideal clock network latency	0.000	8.000		
clock pessimism	0.000	8.000		
clock uncertainty	-0.025	7.975		
output delay	-0.000	7.975		
Required Time		7.975		

Figure 13. First failing path delays for the Zybo

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Compared to delays of Figure 7 (post-synthesis timing report), the net delays are actual delays (rather than the estimated 0.8 ns). The data path delay is less than the destination clock path delay giving a negative slack (violation). The data path delay is 11.940 ns for the ZedBoard, the destination clock path is 9.975 ns and the negative slack is -1.965 ns.

The figures are 10.956 ns, 7.975 ns and -2.981 ns respectively for the Zybo.

At this point we can ignore this violation as the LED display change won't be observable by human eyes.

We can also change the output delay by rounding the negative slack to the nearest whole number (in ns) and make the timings meet.

2-3-5. Select **Implemented Design > Edit Timing Constraints** the *Flow Navigator* pane.

2-3-6. Select the *Set Output Delay* entry in the left pane (under *Outputs*), and change the Delay Value to **-2.000** ns for the ZedBoard or **-3.000** ns for the Zybo.

2-3-7. Click **Apply**.

2-3-8. Click the **Rerun** link (in the yellow notification bar at the bottom of the GUI) to re-run the timing report.

Observe that the timing violations of the Intra-clock paths are gone.

2-3-9. Click on the WNS link; notice the slack is now positive on every one of the paths.

2-3-10. Double-click on the path 23 to see how that is made up of. Also right-click on it and select **Schematic.**

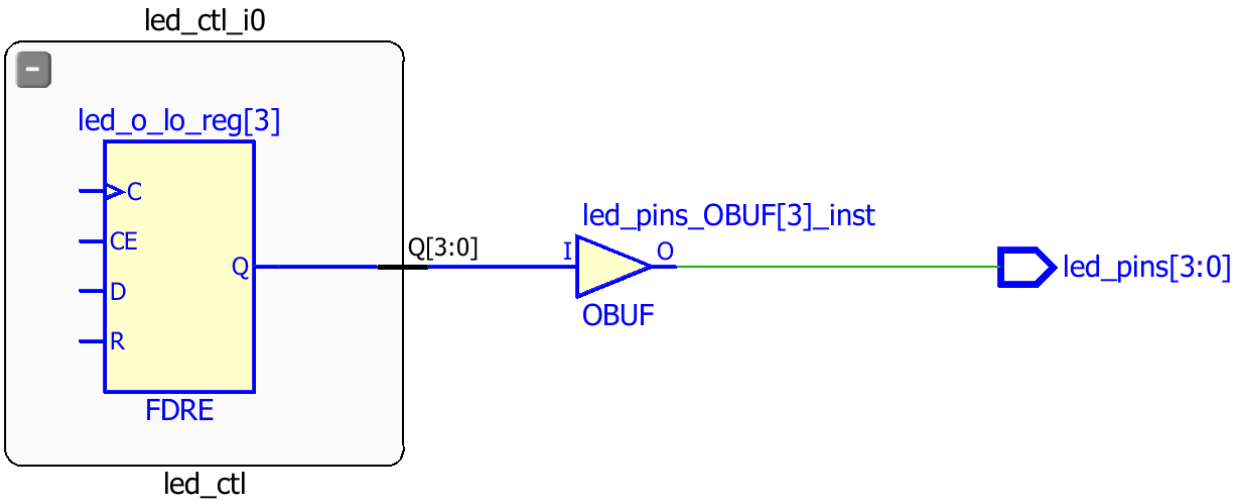

Figure 14. Schematic view of the 10th worst path delay

2-3-11. Click on the **Device** tab and see the highlighted path in the view.

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You may have to zoom-in to see the path.

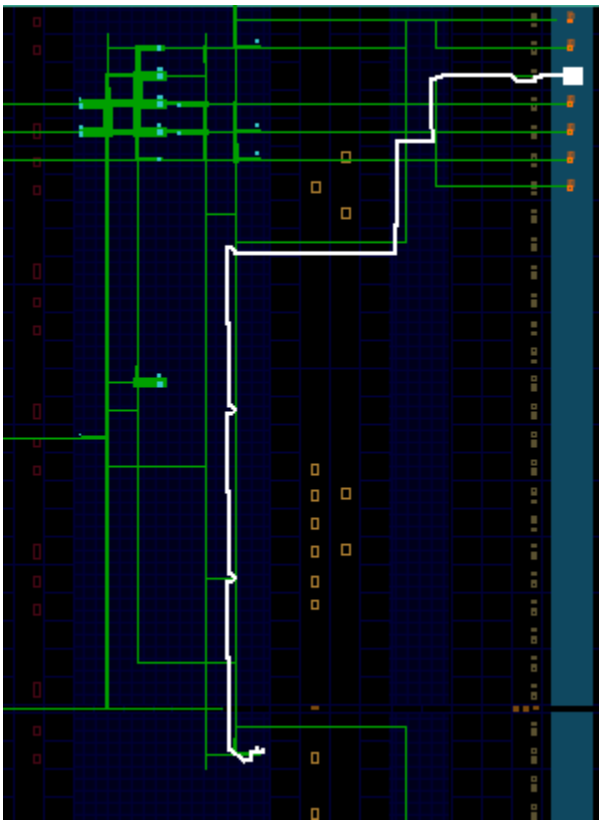

Figure 15. Path displayed in the Device view for the ZedBoard design

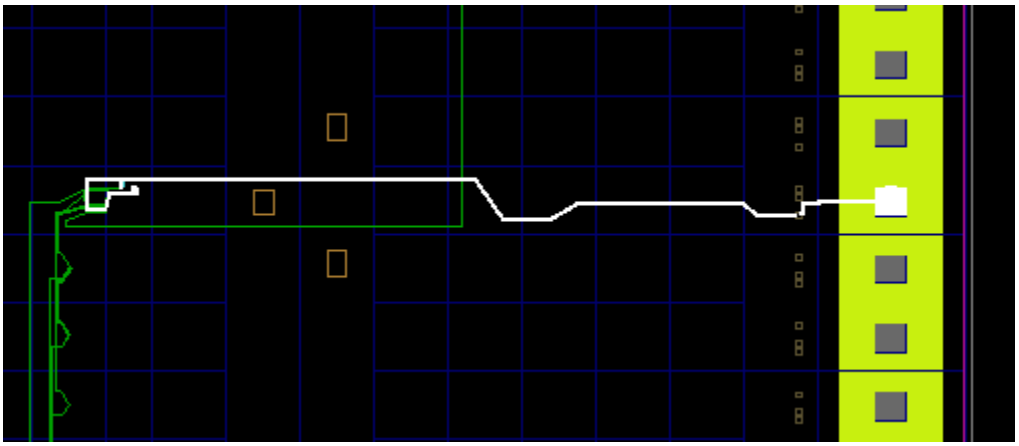

Figure 15. Path displayed in the Device view for the Zybo design

2-3-12. Select **Implemented Design > Report Clock Networks**.

2-3-13. Click **OK**.

The Clock Networks report will be displayed in the Console pane showing two clock net entries.

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2-3-14. Select the *clk_pin* entry and observe the selected nets in the Device view.

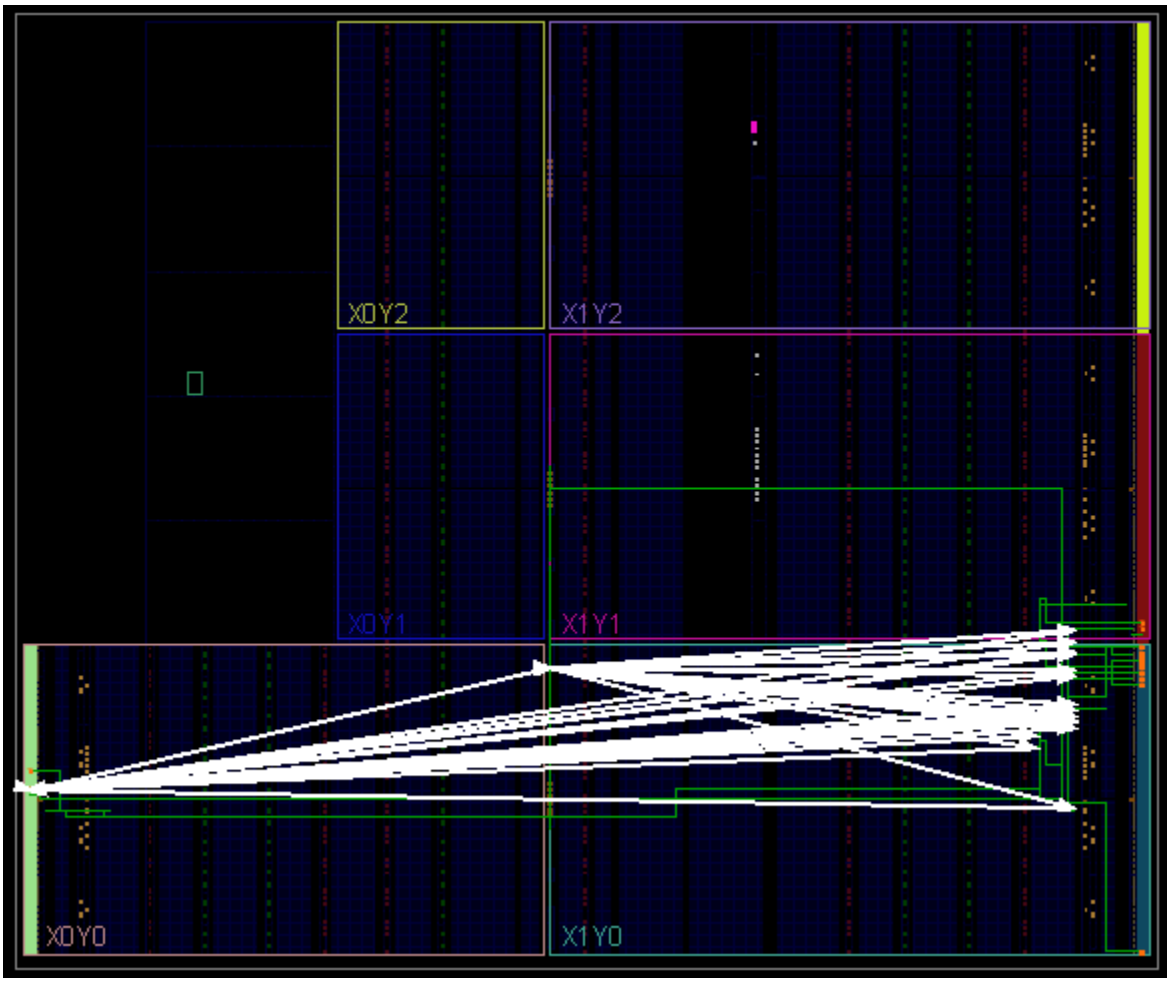

Figure 16. Clock nets for the ZedBoard

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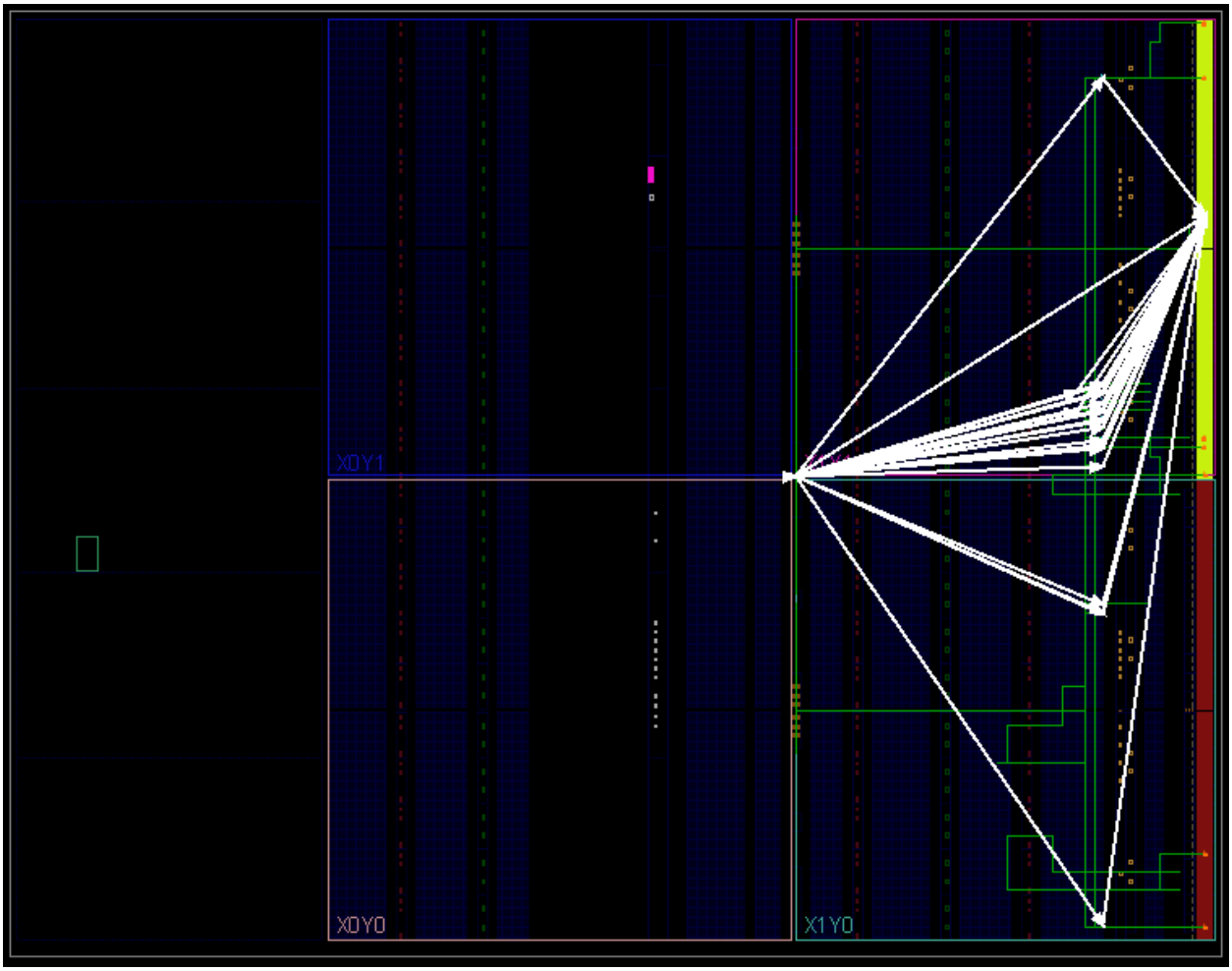

Figure 16. Clock nets for the Zybo

Generate the Bitstream — Step 3

3-1. Generate the bitstream.

3-1-1. In the Flow Navigator, under Program and Debug, click **Generate Bitstream.**

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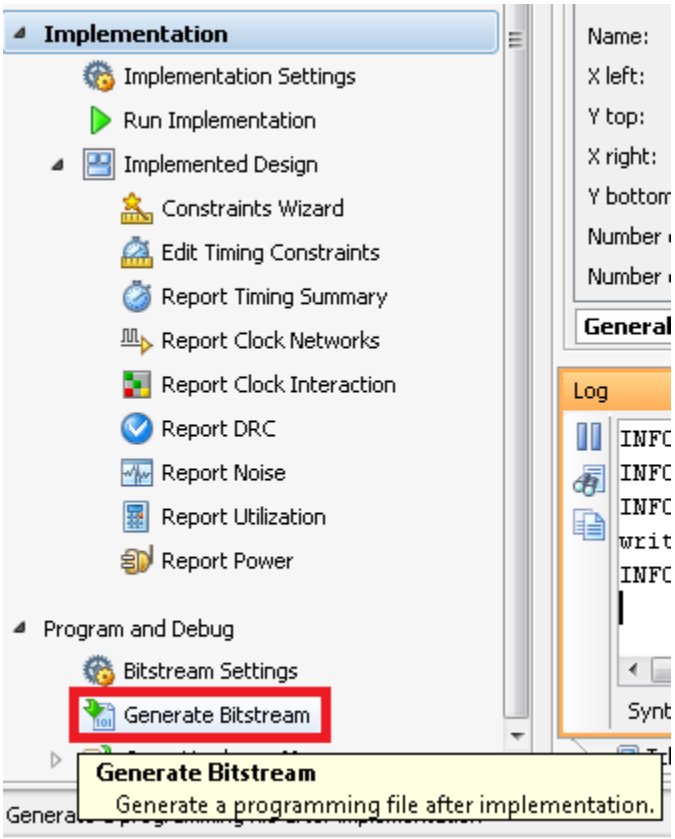

Figure 17, Generating the bitstream

3-1-2. Click **Save** to save the constraints since the timing constraints had been changed and then click **Yes** to reset the runs and re-run all the processes.

3-1-3. The when implementation is complete, the `write_bitstream` command will be executed (you can verify it by looking in the Tcl console).

3-1-4. Click **Cancel** when the bitstream generation is completed.

Verify the Functionality Step 4

4-1. Plug-in the PmodUSBUart module into the top-row of the JA (ZedBoard) or JE (Zybo) PMOD connector. Connect the module to the host machine using a micro-USB cable. Connect the board and power it ON. Open a Hardware Manager, and program the FPGA.

4-1-1. Connect a micro-USB cable between the PmodUSBUart module and the host PC USB port.

4-1-2. Plug-in the PmodUSBUart module into the top-row of the JA PMOD connector for the ZedBoard or the JE PMOD connector for the Zybo.

4-1-3. Make sure that another micro-USB cable is connected to the JTAG PROG connector (next to the power supply switch on both boards). Connect the power jack and turn ON the power.

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4-1-4. Select the *Open Hardware Manager* option and click **OK**.

The Hardware Manager window will open indicating “unconnected” status.

4-1-5. Click on the **Open New Hardware Target** link.

You can also click on the Open Recent Hardware Target link if the board was already targeted before.

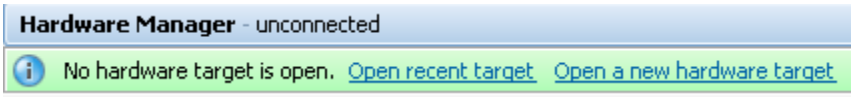

Figure 18. Opening new hardware target

4-1-6. Click **Next** to see the Hardware Server Settings form.

4-1-7. Click **Next** with the Hardware Target selected.

The JTAG cable should be detected and identified as a hardware target. It will also show the hardware devices detected in the chain.

4-1-8. Click **Next** and then **Finish**.

4-1-9. The Hardware Manager status changes from Unconnected to the server name and the device is highlighted. Also notice that the Status indicates that it is not programmed.

4-1-10. Select the device XC7Z020_1 or the XC7Z010_1 in the *Hardware Device Properties,* and verify that the **uart_led.bit** is selected as the programming file in the General tab.

4-2. Start a terminal emulator program such as TeraTerm or HyperTerminal. Select an appropriate COM port (you can find the correct COM number using the Control Panel). Set the COM port for 115200 baud rate communication. Program the FPGA and verify the functionality.

4-2-1. Start a terminal emulator program such as TeraTerm or HyperTerminal.

4-2-2. Select an appropriate COM port (you can find the correct COM number using the Control Panel).

4-2-3. Set the COM port for 115200 baud rate communication.

4-2-4. Right-click on the FPGA entry in the Hardware window and select Program Device.

4-2-5. Click on the Program button.

The programming bit file will be downloaded and the DONE light will be turned ON when the FPGA has been programmed.

4-2-6. Type in some characters in the terminal emulator window and see the corresponding ASCII equivalent bit pattern displayed on the LEDs.

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If the target board is the ZedBoard: The upper and lower four bits will be displayed on the LEDs. Press and hold BTNU and see the the upper four bits are swapped with the lower four bits on the LEDs.

If the target board is the Zybo: Only the lower four bits will be displayed on the LEDs. Press and hold BTN0 to see the upper four bits on the LEDs.

4-2-7. When satisfied, close the terminal emulator program and power OFF the board.

4-2-8. Select **File > Close Hardware Manager**. Click **OK**.

4-2-9. Close the **Vivado** program by selecting **File > Exit** and click **OK**.

Conclusion

In this lab, you learned about many of the reports available to designers in the Vivado IDE. You also had the opportunity to learn basic design analysis using tools that are connected to the display of timing-critical paths, including the Schematic viewer, delay path properties and reports, Device view, and selecting primitive parents. You also learned about the basic timing report options that are at your disposal. You verified the functionality in hardware.

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